UNITED STATES PATENT AND TRADEMARK OFFICE

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>20 August 2009</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>17-26,37 and 38</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>17-26,37 and 38</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>07 July 2006</u> is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 17-26, 37 and 38 have been

considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.　　Determining the scope and contents of the prior art.
2.　　Ascertaining the differences between the prior art and the claims at issue.
3.　　Resolving the level of ordinary skill in the pertinent art.
4.　　Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 17, 19, 20, 22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Marchant; Alan B. (US 6631492 B2) in further view of Nakamura;

Takahiko et al. (US 5684810 A, hereafter referred to as Nakamura) and Kobayashi;

Hisashi et al. (US 6029264 A, hereafter referred to as Kobayashi; Note: Kobayashi is

used strictly as a teaching reference).

Summary of the teachings in Marchant:

Col. 3, lines 30-59 in Marchant teaches using ECC product codeword to correct burst

errors due to scratches. Figures 6 and 7 in Marchant teaches how the ECC product

codeword of Figure 5 lines up with scratches on a recording media prior to being read

and processed to recover the stored data. Note: Col. 4, lines 41-60 in Marchant teaches

that the recorded code is a cross interleaved code so that Figures 5-7 shows how the

inner codewords line up with scratches on a recording media prior to being read and

processed to recover the stored data. Kobayashi is used a a teaching reference for a

cross interleaved code. Figure 2 in the Kobayashi teaching reference teaches that a

cross interleaved codeword is generated by scrambling/interleaving an outer codeword

and inner encoding the scrambled/interleaved outer codeword to generate an inner

codewords as shown in Figure 5-6 of Marchant. Figure 2 in Kobayashi teaches that

deinterleaving occurs after inner decoding a cross interleaved codeword.

35 U.S.C. 103(a) rejection of claims 17 and 22:

Marchant teaches an error correction method for an error correction code (ECC) block

that includes Reed-Solomon-coded data said error correction method using a plurality of

bytes of sub data which comprise error correction codes that are independent from error

correction codes of an error correction target code line to configure erasure position

information (col. 3, lines 30-59 in Marchant teaches using a plurality of pieces of

inner/row codeword sub data which comprise error correction codes that are

independent from error correction codes of an outer/column error correction target code

line to configure erasure position information; Note: col. 3 ,lines 41-57 in Marchant

teaches that inner/row codeword sub data of the product code is used to configure

erasure position information),

the plurality of bytes of sub data including at least a first byte of sub data and a second

byte of sub data (Figure 7 of Marchant teaches that the plurality of bytes of sub data

include at least a first byte of sub data 48b in inner/row codeword sub data row 3 of

Figure 7 and a second byte of sub data 48a in inner/row codeword sub data row 3), said

error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of

main data of the error correction target code line, and a second byte of main data, which

is one of a plurality of bytes of main data of a previous error correction code line, were

located between the first and second bytes of sub data before being deinterleaved (col.

6, lines 28-56 in Marchant teach judging whether or not a first piece of data 48b in

inner/row codeword sub data row 3 of Figure 7, which is one of a plurality of pieces of

data of the outer/column error correction target code line 44b, and a second piece of

data 48a in inner/row codeword sub data row 3, which is one of a plurality of pieces of

data of a previous error correction code line 44a, were located between the same

pieces of inner/row codeword sub data rows 2 to 4 before being deinterleaving; Note:

Col. 4, lines 41-60 in Marchant teaches that the recorded code is a cross interleaved

code so that Figures 5-7 shows how the inner codewords line up with scratches on a

recording media prior to being read and processed to recover the stored data hence

prior to being de-interleaved); configuring erasure position information of said first byte

of main data belonging to the error correction target code line to be identical to erasure

position information of said second byte of main data belonging to the previous error

correction code line when said judging judges that the first byte of main data and the

second byte of main data were both located between the first and second bytes of sub

data before being deinterleaved (col. 6, lines 28-56 in Marchant teach that symbols in a

scratch field are configured/flagged with erasure information for a scratch so that they

are configured/flagged with erasure position information for the same scratch, in

particular; this process is a step for configuring/flagging erasure position information of

said first piece of data 48b belonging to the outer/column error correction target code

line 44b to be the same as identical row position 3 to erasure position information of

said second piece of data 48a belonging to the previous error correction code line 44a

when said judgment step judging judges that the first piece of data 48b and the second

piece of data 48a are both located between the same pieces of inner/row codeword sub

data rows 2 to 4), the erasure position information being obtained at a time of

performing Reed-Solomon decoding on the Reed-Solomon-coded data (Col. 3, lines 41-

47 in Marchant teaches that configuring/flagging with erasure position information

occurs during inner decoding; Note: in cross interleaved codewords, inner decoding

occurs before deinterleaving, e.g., Figure 2 in the Kobayashi teaching reference): and

performing error correction on the error correction target code line (col. 6, lines 28-56 in

Marchant).

As per additional limitations in claim 22: Col. 3, lines 41-47 in Marchant teaches that configuring/flagging with erasure position information occurs during inner decoding prior to de-interleaving.

However Marchant does not explicitly teach the specific use of erasure position information being obtained from a position polynomial.

Nakamura, in an analogous art, teaches the erasure position information being obtained from a position polynomial (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura teaches that during C1 inner decoding error location/position polynomials are generated in Block 3 and are used to generate feedback information to generate erasure information in Blocks 7, 7(b), 7(c) and 8; specifically, col. 7, lines 2-5 in Nakamura teaches that error locations of the C1 error location/position polynomial are converted to erasure locations whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, that is; the erasure position/location information stored in Block 8 is obtained from a error/position polynomial)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant with the teachings of Nakamura by including use of erasure position information being obtained from a position polynomial. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of erasure position information being obtained from a position polynomial would have provided a means for obtaining erasure information for inner C1 uncorrectable errors (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura).

35 U.S.C. 103(a) rejection of claims 19 and 24:

Marchant teaches an error correction method for an error correction code (ECC) block

that includes Reed-Solomon-coded data said error correction method using a plurality of

bytes of sub data which comprise error correction codes that are independent from error

correction codes of an error correction target code line to configure erasure position

information (col. 3, lines 30-59 in Marchant teaches using a plurality of pieces of

inner/row codeword sub data which comprise error correction codes that are

independent from error correction codes of an outer/column error correction target code

line to configure erasure position information; Note: col. 3 ,lines 41-57 in Marchant

teaches that inner/row codeword sub data of the product code is used to configure

erasure position information),

the plurality of bytes of sub data including at least a first byte of sub data and a second

byte of sub data (Figure 7 of Marchant teaches that the plurality of bytes of sub data

include at least a first byte of sub data 48b in inner/row codeword sub data row 3 of

Figure 7 and a second byte of sub data 48a in inner/row codeword sub data row 3), said

error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of

main data of the error correction target code line, and a second byte of main data, which

is one of a plurality of bytes of main data of a previous error correction code line, were

located between the first and second bytes of sub data before being deinterleaved (col.

6, lines 28-56 in Marchant teach judging whether or not a first piece of data 48b in

inner/row codeword sub data row 3 of Figure 7, which is one of a plurality of pieces of

data of the outer/column error correction target code line 44b, and a second piece of

data 48a in inner/row codeword sub data row 3, which is one of a plurality of pieces of

data of a previous error correction code line 44a, were located between the same

pieces of inner/row codeword sub data rows 2 to 4 before being deinterleaving; Note:

Col. 4, lines 41-60 in Marchant teaches that the recorded code is a cross interleaved

code so that Figures 5-7 shows how the inner codewords line up with scratches on a

recording media prior to being read and processed to recover the stored data hence

prior to being de-interleaved); configuring erasure position information of said first byte

of main data belonging to the error correction target code line to be identical to erasure

position information of said second byte of main data belonging to the previous error

correction code line when said judging judges that the first byte of main data and the

second byte of main data were both located between the first and second bytes of sub

data before being deinterleaved (col. 6, lines 28-56 in Marchant teach that symbols in a

scratch field are configured/flagged with erasure information for a scratch so that they

are configured/flagged with erasure position information for the same scratch, in

particular; this process is a step for configuring/flagging erasure position information of

said first piece of data 48b belonging to the outer/column error correction target code

line 44b to be the same as identical row position 3 to erasure position information of

said second piece of data 48a belonging to the previous error correction code line 44a

when said judgment step judging judges that the first piece of data 48b and the second

piece of data 48a are both located between the same pieces of inner/row codeword sub

data rows 2 to 4), the erasure position information being obtained at a time of

performing Reed-Solomon decoding on the Reed-Solomon-coded data (Col. 3, lines 41-

47 in Marchant teaches that configuring/flagging with erasure position information

occurs during inner decoding; Note: in cross interleaved codewords, inner decoding

occurs before deinterleaving, e.g., Figure 2 in the Kobayashi teaching reference): and

performing error correction on the error correction target code line (col. 6, lines 28-56 in

Marchant).

As per additional limitations in claim 24: Col. 3, lines 41-47 in Marchant teaches that

configuring/flagging with erasure position information occurs during inner decoding prior

to de-interleaving.

However Marchant does not explicitly teach the specific use of erasure position

information being obtained from a position polynomial.

Nakamura, in an analogous art, teaches the erasure position information being obtained

from a position polynomial (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura

teaches that during C1 inner decoding error location/position polynomials are generated

in Block 3 and are used to generate feedback information to generate erasure

information in Blocks 7, 7(b), 7(c) and 8; specifically, col. 7, lines 2-5 in Nakamura

teaches that error locations of the C1 error location/position polynomial are converted to

erasure locations whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c)

and 8, that is; the erasure position/location information stored in Block 8 is obtained

from a error/position polynomial)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Marchant with the teachings of Nakamura by including

use of erasure position information being obtained from a position polynomial. This

modification would have been obvious to one of ordinary skill in the art, at the time the

invention was made, because one of ordinary skill in the art would have recognized that

use of erasure position information being obtained from a position polynomial would

have provided a means for obtaining erasure information for inner C1 uncorrectable

errors (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura).

Sub data 48a and 48b in Figure 7 of Marchant is sync data for configuring/flagging

erasures.

35 U.S.C. 102(e) rejection of claims 20 and 25.

If first data is outside of sub data 48a and 48b in Figured 7 of Marchant, then it does not

exist within sub data 48a and 48b.

Claims 18, 23, 37 and 38 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Marchant; Alan B. (US 6631492 B2) in further view of Nakamura;

Takahiko et al. (US 5684810 A, hereafter referred to as Nakamura) and Kobayashi;

Hisashi et al. (US 6029264 A, hereafter referred to as Kobayashi; Note: Kobayashi is

used strictly as a teaching reference) in further view of Shutoku; Toshiyuki et al. (US

7089401 B2, hereafter referred to as Shutoku).

35 U.S.C. 103(a) rejection of claims 18 and 23.

Marchant teaches an error correction method for an error correction code (ECC) block

that includes Reed-Solomon-coded data said error correction method using a plurality of

bytes of sub data which comprise error correction codes that are independent from error

correction codes of an error correction target code line to configure erasure position

information (col. 3, lines 30-59 in Marchant teaches using a plurality of pieces of

inner/row codeword sub data which comprise error correction codes that are

independent from error correction codes of an outer/column error correction target code

line to configure erasure position information; Note: col. 3 ,lines 41-57 in Marchant

teaches that inner/row codeword sub data of the product code is used to configure

erasure position information),

the plurality of bytes of sub data including at least a first byte of sub data and a second

byte of sub data (Figure 7 of Marchant teaches that the plurality of bytes of sub data

include at least a first byte of sub data 48b in inner/row codeword sub data row 3 of

Figure 7 and a second byte of sub data 48a in inner/row codeword sub data row 3), said

error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of

main data of the error correction target code line, and a second byte of main data, which

is one of a plurality of bytes of main data of a previous error correction code line, were

located between the first and second bytes of sub data before being deinterleaved (col.

6, lines 28-56 in Marchant teach judging whether or not a first piece of data 48b in

inner/row codeword sub data row 3 of Figure 7, which is one of a plurality of pieces of

data of the outer/column error correction target code line 44b, and a second piece of

data 48a in inner/row codeword sub data row 3, which is one of a plurality of pieces of

data of a previous error correction code line 44a, were located between the same

pieces of inner/row codeword sub data rows 2 to 4 before being deinterleaving; Note:

Col. 4, lines 41-60 in Marchant teaches that the recorded code is a cross interleaved

code so that Figures 5-7 shows how the inner codewords line up with scratches on a

recording media prior to being read and processed to recover the stored data hence

prior to being de-interleaved); configuring erasure position information of said first byte

of main data belonging to the error correction target code line to be identical to erasure

position information of said second byte of main data belonging to the previous error

correction code line when said judging judges that the first byte of main data and the

second byte of main data were both located between the first and second bytes of sub

data before being deinterleaved (col. 6, lines 28-56 in Marchant teach that symbols in a

scratch field are configured/flagged with erasure information for a scratch so that they

are configured/flagged with erasure position information for the same scratch, in

particular; this process is a step for configuring/flagging erasure position information of

said first piece of data 48b belonging to the outer/column error correction target code

line 44b to be the same as identical row position 3 to erasure position information of

said second piece of data 48a belonging to the previous error correction code line 44a

when said judgment step judging judges that the first piece of data 48b and the second

piece of data 48a are both located between the same pieces of inner/row codeword sub

data rows 2 to 4), the erasure position information being obtained at a time of

performing Reed-Solomon decoding on the Reed-Solomon-coded data (Col. 3, lines 41-

47 in Marchant teaches that configuring/flagging with erasure position information

occurs during inner decoding; Note: in cross interleaved codewords, inner decoding

occurs before deinterleaving, e.g., Figure 2 in the Kobayashi teaching reference): and

performing error correction on the error correction target code line (col. 6, lines 28-56 in

Marchant).

As per additional limitations in claim 23: Col. 3, lines 41-47 in Marchant teaches that

configuring/flagging with erasure position information occurs during inner decoding prior

to de-interleaving.

However Marchant does not explicitly teach the specific use of erasure position

information being obtained from a position polynomial.

Nakamura, in an analogous art, teaches the erasure position information being obtained

from a position polynomial (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura

teaches that during C1 inner decoding error location/position polynomials are generated

in Block 3 and are used to generate feedback information to generate erasure

information in Blocks 7, 7(b), 7(c) and 8; specifically, col. 7, lines 2-5 in Nakamura

teaches that error locations of the C1 error location/position polynomial are converted to

erasure locations whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c)

and 8, that is; the erasure position/location information stored in Block 8 is obtained

from a error/position polynomial)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Marchant with the teachings of Nakamura by including

use of erasure position information being obtained from a position polynomial. This

modification would have been obvious to one of ordinary skill in the art, at the time the

invention was made, because one of ordinary skill in the art would have recognized that

use of erasure position information being obtained from a position polynomial would

have provided a means for obtaining erasure information for inner C1 uncorrectable

errors (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura).

However Marchant does not explicitly teach the specific use of a typical DVD recording

data structure as encompassed in the language "wherein the ECC block includes a

plurality of main data areas comprising the plurality of bytes of main data of the error

correction target code line and the plurality of bytes of main data of the previous error

correction target code line, and a plurality of sub data areas comprising the plurality of

bytes of sub data, wherein the plurality of main data areas include a first main data area

and a second main data area, wherein the plurality of sub data areas include: a first sub

data area in which the first byte of sub data is located; a second sub data area in which

the second byte of sub data is located; and a third sub data area in which a third byte of

sub data is located, wherein the first main data area is disposed between the first sub

data area and the second sub data area, wherein the second main data area is

disposed between the second sub data area and the third sub data area wherein the

second sub data area is disposed between the first main data area and the second

main data area, and wherein said error correction target code line extends so as to be

located in both of the first and second main data areas of the ECC block".

Shutoku, in an analogous art, teaches use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block" (Figure 1-3 and col. 8, lines 52-55 in Shutoku).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant with the teachings of Shutoku by including use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas

comprising the plurality of bytes of sub data, wherein the plurality of main data areas

include a first main data area and a second main data area, wherein the plurality of sub

data areas include: a first sub data area in which the first byte of sub data is located; a

second sub data area in which the second byte of sub data is located; and a third sub

data area in which a third byte of sub data is located, wherein the first main data area is

disposed between the first sub data area and the second sub data area, wherein the

second main data area is disposed between the second sub data area and the third sub

data area wherein the second sub data area is disposed between the first main data

area and the second main data area, and wherein said error correction target code line

extends so as to be located in both of the first and second main data areas of the ECC

block". This modification would have been obvious to one of ordinary skill in the art, at

the time the invention was made, because one of ordinary skill in the art would have

recognized that use of a typical DVD recording data structure as encompassed in the

language "wherein the ECC block includes a plurality of main data areas comprising the

plurality of bytes of main data of the error correction target code line and the plurality of

bytes of main data of the previous error correction target code line, and a plurality of sub

data areas comprising the plurality of bytes of sub data, wherein the plurality of main

data areas include a first main data area and a second main data area, wherein the

plurality of sub data areas include: a first sub data area in which the first byte of sub

data is located; a second sub data area in which the second byte of sub data is located;

and a third sub data area in which a third byte of sub data is located, wherein the first

main data area is disposed between the first sub data area and the second sub data

area, wherein the second main data area is disposed between the second sub data

area and the third sub data area wherein the second sub data area is disposed between

the first main data area and the second main data area, and wherein said error

correction target code line extends so as to be located in both of the first and second

main data areas of the ECC block" would have provided scratch protection for DVDs.

35 U.S.C. 103(a) rejection of claims 37 and 38.

Marchant teaches an error correction method for an error correction code (ECC) block

that includes Reed-Solomon-coded data said error correction method using a plurality of

bytes of sub data which comprise error correction codes that are independent from error

correction codes of an error correction target code line to configure erasure position

information (col. 3, lines 30-59 in Marchant teaches using a plurality of pieces of

inner/row codeword sub data which comprise error correction codes that are

independent from error correction codes of an outer/column error correction target code

line to configure erasure position information; Note: col. 3 ,lines 41-57 in Marchant

teaches that inner/row codeword sub data of the product code is used to configure

erasure position information),

the plurality of bytes of sub data including at least a first byte of sub data and a second

byte of sub data (Figure 7 of Marchant teaches that the plurality of bytes of sub data

include at least a first byte of sub data 48b in inner/row codeword sub data row 3 of

Figure 7 and a second byte of sub data 48a in inner/row codeword sub data row 3), said

error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of

main data of the error correction target code line, and a second byte of main data, which

is one of a plurality of bytes of main data of a previous error correction code line, were

located between the first and second bytes of sub data before being deinterleaved (col.

6, lines 28-56 in Marchant teach judging whether or not a first piece of data 48b in

inner/row codeword sub data row 3 of Figure 7, which is one of a plurality of pieces of

data of the outer/column error correction target code line 44b, and a second piece of

data 48a in inner/row codeword sub data row 3, which is one of a plurality of pieces of

data of a previous error correction code line 44a, were located between the same

pieces of inner/row codeword sub data rows 2 to 4 before being deinterleaving; Note:

Col. 4, lines 41-60 in Marchant teaches that the recorded code is a cross interleaved

code so that Figures 5-7 shows how the inner codewords line up with scratches on a

recording media prior to being read and processed to recover the stored data hence

prior to being de-interleaved); configuring erasure position information of said first byte

of main data belonging to the error correction target code line to be identical to erasure

position information of said second byte of main data belonging to the previous error

correction code line when said judging judges that the first byte of main data and the

second byte of main data were both located between the first and second bytes of sub

data before being deinterleaved (col. 6, lines 28-56 in Marchant teach that symbols in a

scratch field are configured/flagged with erasure information for a scratch so that they

are configured/flagged with erasure position information for the same scratch, in

particular; this process is a step for configuring/flagging erasure position information of

said first piece of data 48b belonging to the outer/column error correction target code

line 44b to be the same as identical row position 3 to erasure position information of

said second piece of data 48a belonging to the previous error correction code line 44a

when said judgment step judging judges that the first piece of data 48b and the second

piece of data 48a are both located between the same pieces of inner/row codeword sub

data rows 2 to 4), the erasure position information being obtained at a time of

performing Reed-Solomon decoding on the Reed-Solomon-coded data (Col. 3, lines 41-

47 in Marchant teaches that configuring/flagging with erasure position information

occurs during inner decoding; Note: in cross interleaved codewords, inner decoding

occurs before deinterleaving, e.g., Figure 2 in the Kobayashi teaching reference): and

performing error correction on the error correction target code line (col. 6, lines 28-56 in

Marchant).

Sub data 48a and 48b in Figure 7 of Marchant is sync data for configuring/flagging

erasures.

As per additional limitations in claim 38: Col. 3, lines 41-47 in Marchant teaches that

configuring/flagging with erasure position information occurs during inner decoding prior

to de-interleaving.

However Marchant does not explicitly teach the specific use of erasure position

information being obtained from a position polynomial.

Nakamura, in an analogous art, teaches the erasure position information being obtained

from a position polynomial (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura

teaches that during C1 inner decoding error location/position polynomials are generated

in Block 3 and are used to generate feedback information to generate erasure

information in Blocks 7, 7(b), 7(c) and 8; specifically, col. 7, lines 2-5 in Nakamura

teaches that error locations of the C1 error location/position polynomial are converted to

erasure locations whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c)

and 8, that is; the erasure position/location information stored in Block 8 is obtained

from a error/position polynomial)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Marchant with the teachings of Nakamura by including

use of erasure position information being obtained from a position polynomial. This

modification would have been obvious to one of ordinary skill in the art, at the time the

invention was made, because one of ordinary skill in the art would have recognized that

use of erasure position information being obtained from a position polynomial would

have provided a means for obtaining erasure information for inner C1 uncorrectable

errors (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura).

However Marchant does not explicitly teach the specific use of a typical DVD recording

data structure as encompassed in the language "wherein the ECC block includes a

plurality of main data areas comprising the plurality of bytes of main data of the error

correction target code line and the plurality of bytes of main data of the previous error

correction target code line, and a plurality of sub data areas comprising the plurality of

bytes of sub data, wherein the plurality of main data areas include a first main data area

and a second main data area, wherein the plurality of sub data areas include: a first sub

data area in which the first byte of sub data is located; a second sub data area in which

the second byte of sub data is located; and a third sub data area in which a third byte of

sub data is located, wherein the first main data area is disposed between the first sub

data area and the second sub data area, wherein the second main data area is

disposed between the second sub data area and the third sub data area wherein the

second sub data area is disposed between the first main data area and the second

main data area, and wherein said error correction target code line extends so as to be

located in both of the first and second main data areas of the ECC block".

Shutoku, in an analogous art, teaches use of a typical DVD recording data structure as

encompassed in the language "wherein the ECC block includes a plurality of main data

areas comprising the plurality of bytes of main data of the error correction target code

line and the plurality of bytes of main data of the previous error correction target code

line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second

main data area, wherein the plurality of sub data areas include: a first sub data area in

which the first byte of sub data is located; a second sub data area in which the second

byte of sub data is located; and a third sub data area in which a third byte of sub data is

located, wherein the first main data area is disposed between the first sub data area

and the second sub data area, wherein the second main data area is disposed between

the second sub data area and the third sub data area wherein the second sub data area

is disposed between the first main data area and the second main data area, and

wherein said error correction target code line extends so as to be located in both of the

first and second main data areas of the ECC block" (Figure 1-3 and col. 8, lines 52-55 in

Shutoku).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Marchant with the teachings of Shutoku by including use

of a typical DVD recording data structure as encompassed in the language "wherein the

ECC block includes a plurality of main data areas comprising the plurality of bytes of

main data of the error correction target code line and the plurality of bytes of main data

of the previous error correction target code line, and a plurality of sub data areas

comprising the plurality of bytes of sub data, wherein the plurality of main data areas

include a first main data area and a second main data area, wherein the plurality of sub

data areas include: a first sub data area in which the first byte of sub data is located; a

second sub data area in which the second byte of sub data is located; and a third sub

data area in which a third byte of sub data is located, wherein the first main data area is

disposed between the first sub data area and the second sub data area, wherein the

second main data area is disposed between the second sub data area and the third sub

data area wherein the second sub data area is disposed between the first main data

area and the second main data area, and wherein said error correction target code line

extends so as to be located in both of the first and second main data areas of the ECC

block". This modification would have been obvious to one of ordinary skill in the art, at

the time the invention was made, because one of ordinary skill in the art would have

recognized that use of a typical DVD recording data structure as encompassed in the

language "wherein the ECC block includes a plurality of main data areas comprising the

plurality of bytes of main data of the error correction target code line and the plurality of

bytes of main data of the previous error correction target code line, and a plurality of sub

data areas comprising the plurality of bytes of sub data, wherein the plurality of main

data areas include a first main data area and a second main data area, wherein the

plurality of sub data areas include: a first sub data area in which the first byte of sub

data is located; a second sub data area in which the second byte of sub data is located;

and a third sub data area in which a third byte of sub data is located, wherein the first

main data area is disposed between the first sub data area and the second sub data

area, wherein the second main data area is disposed between the second sub data

area and the third sub data area wherein the second sub data area is disposed between

the first main data area and the second main data area, and wherein said error

correction target code line extends so as to be located in both of the first and second

main data areas of the ECC block" would have provided scratch protection for DVDs.

Claims 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Marchant; Alan B. (US 6631492 B2) in further view of Nakamura; Takahiko et al.

(US 5684810 A, hereafter referred to as Nakamura) and Kobayashi; Hisashi et al. (US

6029264 A, hereafter referred to as Kobayashi; Note: Kobayashi is used strictly as a

teaching reference) in further view of Eachus; Joseph J. (US 3685016 A).

35 U.S.C. 103(a) rejection of claims 21 and 26.

Marchant and Nakamura substantially teaches the claimed invention described in

claims 17-20, 22-25, 27-30 and 32-35 (as rejected above).

However Marchant and Nakamura does not explicitly teach the specific use of avoiding

error correction when error correction capabilities are exceeded.

Eachus, in an analogous art, teaches use of avoiding error correction when error

correction capabilities are exceeded (col. 13, lines 1-10 in Eachus).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Marchant and Nakamura with the teachings of Eachus by

including use of avoiding error correction when error correction capabilities are

exceeded. This modification would have been obvious to one of ordinary skill in the art,

at the time the invention was made, because one of ordinary skill in the art would have

recognized that use of avoiding error correction when error correction capabilities are

exceeded would have provided means for avoiding meaningless calculations (col. 13,

lines 1-10 in Eachus).

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Joseph D. Torres whose telephone number is (571)

272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Scott T. Baderman can be reached on (571) 272-3644. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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